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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/024,101	12/17/2001	Tracy Kristine Ragland	10011126-1	5192

7590 03/11/2004

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EXAMINER	
SUN, XIUQIN	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/024,101	RAGLAND, TRACY KRISTINE	
	Examiner	Art Unit	
	Xiuqin Sun	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-19,21-24,26,27,29-36 and 38-47* is/are rejected.

7)☒ Claim(s) *8,20,25,28 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7, 11-19, 23, 24, 26, 27, 29-35 and 38-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams et al. (U.S. Pat. No. RE35423) in view of Cannon (U.S. Pat. No. 6580501) and Yamamura et al. (U.S. Pat. No. 5780866).

Adams et al. teach a method for adapting test thresholds, comprising the following steps: acquiring location information for a plurality of solder joints on a printed-circuit device (col. 6, lines 57-67; col. 7, lines 1-4; col. 9, lines 56-67 and col. 10, lines 1-12); recording a measurement of a physical property of a plurality of solder joints used to couple the printed-circuit device to the printed-circuit board (col. 12, lines 12-32); estimating a range of acceptable measurements for respective solder joints (col. 12, lines 12-32); and setting at least one threshold responsive to the range (col. 12, lines 12-32). Adams et al. also teach: said step of acquiring location information comprises an investigation of an array package (col. 12, lines 33-52); said step of recording comprises a diameter measurement (col. 13, lines 57-67 and col. 14, lines 1-3); said step of recording comprises a volume measurement (col. 16, lines 38-46); comparing the expected value with the recorded measurement to generate an error

value for the plurality of solder joints on the printed-circuit device, including a mathematical combination (such as a difference or an error) of the expected value with the recorded measurement (col. 12, lines 33-52 and co. 13, lines 16-26); and performing an outlier analysis on the plurality of error values to establish at least one threshold value (col. 12, lines 33-52 and co. 13, lines 16-26). Adams et al. further teach a method for identifying solder joint defects, comprising the steps of: recording a measurement associated with a plurality of solder joints on a printed circuit device (col. 12, lines 12-32); estimating an expected value for the plurality of solder joints that accounts for acceptable variance of certain characteristics within various solder-joints (col. 12, lines 12-32); comparing the recorded measurement with the expected value for the plurality of solder joints to generate a respective error value (col. 12, lines 33-52 and co. 13, lines 16-26); and identifying defective solder joints by applying an error value outlier analysis to the plurality of error values (col. 12, lines 33-52 and co. 13, lines 16-26); said step of estimating an expected value for the plurality of solder joints comprises performing a statistical analysis on the recorded measurements of a set of solder joints equidistant from the centroid of the printed-circuit device (col. 12, lines 53-67; co. 13, lines 1-15 and col. 14, lines 35-46). Adams et al. further teach a solder-joint inspection system and a solder-joint defect analysis detection program, comprising: means for measuring at least one characteristic of a plurality of solder joints on a printed-circuit device (col. 6, lines 57-67 and col. 7, lines 1-4); means for computing an expected value for the measured characteristic for each of the plurality of solder joints that varies as a function of a second characteristics of a plurality of solder joints (col. 12, lines 12-32);

and means for formulating an error value as a function of the measured characteristic and the expected value for the plurality of solder joints (col. 12, lines 33-52 and co. 13, lines 16-26). Adams et al. further teach the means of: analyzing the plurality of error values to identify solder joint defects (col. 12, lines 12-32); said means for measuring comprises an automated X-ray inspection system (col. 4, lines 60-67 and co. 5, lines 1-12); said means for measuring comprises an optical inspection system (col. 23, lines 2-32); and said step of recording comprises a one dimension or two dimensional measurement (col. 3, lines 25-54).

Adams et al. do not mention explicitly that: obtaining information indicative of the variation in distance between a mounting surface of the printed-circuit device and a printed-circuit board; analyzing recorded measurements of a set of neighbor solder joints to calculate a range of acceptable measurements for each respective neighbor solder joint responsive to said variation; said step of acquiring location information comprises an investigation of a quad flat pack package; sad step of recording comprises a three dimensional measurement; estimating an expected value for the plurality of solder joints that accounts for acceptable variance in the distance between the mounting surfaces of a printed-circuit device and a printed-circuit board coupled by the solder joints; said step of recording comprises a height measurement; and said measurements and analysis are performed on a plurality of solder joints located within a selected area of a printed-circuit device.

Cannon discloses a method and system for inspection in particular of soldered joints, and teaches the step and means of obtaining information indicative of the

variation in distance between a mounting surface of the printed-circuit device and a printed-circuit board, and inspecting the quality of respective soldered joints responsive to variation in distance between the mounting surface of the printed-circuit device and the printed-circuit board (col. 6, lines 36-59). Cannon further teaches: said method and system comprises the step and means of height measurement (col. 2, lines 57-67).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teachings of Cannon in the invention of Adams et al. in order to use the gap height between the mounting surface of the printed-circuit device and the printed-circuit board to measure the quality of soldered joints (Cannon, col. 6, lines 36-59).

Yamamura et al. disclose a method and apparatus for three dimensional profile detection, and teach the step and means of: analyzing recorded measurements of a set of neighbor solder joints to calculate a range of acceptable measurements for each respective neighbor solder joint responsive to variation in height of the surface of a part-mounted board, wherein said measurements and analysis are performed on a plurality of solder joints located within a selected area of said board (cols. 5-6, lines 50-42; and cols. 8-9, lines 33-29).Yamamura et al. further teach: the step and means of acquiring location information comprises an investigation of a quad flat pack package (col. 12, lines 22-29, col. 16, lines 66-67; col. 17, lines 1-21 and col. 23, lines 8-24); and the step and means of recording comprises a three dimensional measurement (see Abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teachings of Yamamura et al. in the combination of

Adams et al. and Cannon in order to examine the regional characteristics of the quality of a plurality of solder joints from a three dimensional profile signal (Yamamura et al., Abstract).

As per claims 7, 19 and 34, it would have been obvious to one having ordinary skill in the art at the time the invention was made that calculating a median of an identified set of neighboring samples is a well-known common practice of a statistical analysis on the set of neighboring samples, in this case, an identified set of neighbor solder joints.

3. Claims 9, 10, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams et al. in view of Cannon and Yamamura et al., as applied to claims 1 and 14 above, and further in view of Chang et al. (U.S. Pat. No. 4792683).

Adams et al., Cannon and Yamamura et al. teach a method and system that includes the subject matter discussed above. The combination of Adams et al., Cannon and Yamamura et al. do not mention: said estimating step comprises applying the recorded measurements of a plurality of solder joints in a Fourier analysis; said Fourier analysis comprises the application of a high-frequency filter on the recorded measurements of an identified set of solder joints distributed across the surface of the device.

Chang et al. teach the step and means of: applying the recorded measurements of a plurality of solder joints in a Fourier analysis (col. 2, lines 64-67; col. 5, lines 8-34; col. 7, lines 60-67 and col.8, lines 1-24); said Fourier analysis comprises the application

of a high-frequency filter on the recorded measurements of an identified set of solder joints distributed across the surface of the device (col. 4, lines 11-20)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teachings of Chang et al. in the combination of Adams et al., Cannon and Yamamura et al. in order to examine the integrity and spatial variability of a plurality of solder joints distributed across the surface of the device (Chang et al., Abstract).

Allowable Subject Matter

4. Claims 8, 20, 25, 28, 36 and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

5. The following is an examiner's statement of reasons for allowance:

The primary reason for the allowance of claims 8 and 20 is the claimed method step of formulating a best fit polynomial equation using the recorded measurements of a plurality of solder joints. It is this step found in each of the claims, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes these claims allowable over the prior art.

The primary reason for the allowance of claims 25, 28, 36 and 37 is the claimed step and means of identifying defective solder joints comprises a box plot analysis

responsive to the plurality of error values. It is this limitation found in each of the claims, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes these claims allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

6. Applicant's arguments with respect to claims 1-7, 9-19, 21-24, 26, 27, 29-35 and 38-47 have been considered but are moot in view of the new ground(s) of rejection.

Claims 1-7, 9-19, 21-24, 26, 27, 29-35 are rejected as new grounds of rejection from the Yamamura patent (U.S. Pat. No. 5780866 to Yamamura et al.) have been found to teach the step and means of analyzing recorded measurements of a set of neighbor solder joints to calculate a range of acceptable measurements for each respective neighbor solder joint responsive to variation in the height of a part-mounted board surface, wherein said measurements and analysis are performed on a plurality of solder joints located within a selected area of said board. For more detailed discussion, please refer to section 2 set forth above in this Office Action.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiuqin Sun whose telephone number is (571)272-2280. The examiner can normally be reached on 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571)272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Xiuqin Sun
Examiner
Art Unit 2863

XS

March 2, 2004

John Barlow
Supervisory Patent Examiner
Technology Center 2800

XS
March 2, 2004